A Coplanar-to-Microstrip Transition for W-Band Circuit Fabrication with 100-μm-Thick GaAs Wafers

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***Abstract*—Results on a via-hole interconnect that links a coplanar waveguide (CPW) on one side of a 100-mm thick GaAs substrate to a microstrip line on the opposite side are presented. The measured insertion loss of a pair of back-to-back connections is 0.3 dB between 26.5 and 40 GHz. A lumped-element equivalent circuit of this via-hole interconnect has been extrapolated to W-band and used to design amplifiers at 94 GHz.**

I. Introduction

MICROSTRIP is the preferred transmission medium of choice in most MMIC designs because it is well characterized and has reasonable loss and dispersion for most applications. However, as operating frequencies approach 100 GHz, microstrip suffers from several limitations [1]. In particular, its coupling to FET's is increasingly limited by the parasitics associated with the junction of device and transmission line. It becomes increasingly difficult to address this problem with microstrip layouts as the frequency is raised.

A second significant problem emerges because the FET and the microstrip ground plane are on opposite sides of the substrate. Since most applications require one of the device's three terminals to be common to both the input and output ports, it is necessary to bring the ground plane to the same side as the device. This is conveniently done with via holes [2], [3]. However, as the frequency is increased, via hole inductance becomes significant and reduces device gain through negative feedback. This inductance may be reduced by thinning the wafer to 50 μm for W-band circuits, but there are drawbacks: 1) the wafer becomes difficult to handle, with consequent loss of yield; and 2) RF losses in the microstrip lines increase.

We eliminated these problems by placing the active device in a coplanar waveguide (CPW) line and designing its layout such that the electron transport and the CPW electric field are colinear. This procedure maximizes coupling to the device and significantly reduces parasitics. Moreover, the ground plane is on the same surface as the device which eliminates the need for via holes in the common terminal.

However, CPW circuit elements such as stubs, gaps, steps, tees and crosses are not as well known as the corresponding microstrip elements. Consequently, we fabricated these circuit elements, measured them at Ka-band and developed models to predict their behavior at W-band. We then combined CPW and microstrip environments in our W-band approach, enabling the strengths of each to be exploited. This letter focuses on the CPW-to- microstrip transition and presents the results of our on-wafer Ka-band measurements. This approach was successfully employed to fabricate a W-band amplifier.

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II. Process

The process used for the fabrication of the CPW-to-microstrip transition is completely compatible with GaAs MMIC processing. As a result, it can be immediately inserted into an established process with only some additional steps required for backside processing.

All wafers were ⟨100⟩, 2-inch-diameter, semi-insulating GaAs. The first step comprises deposition of the electroplating base and definition of the coplanar environment on the front side of the wafer with standard photolithography. The wafer is then electroplated with 4 μm of Au via pulse plating (10% duty cycle). At this point, the wafer is thinned to 100 μm and via holes are patterned and etched through the substrate with a reactive ion etch process based on CCl_2F_2. In a conventional MMIC in a microstrip environment, the back of the wafer is uniformly plated. However, in our process, the microstrip is defined on the backside after the via holes are etched and is then electroplated selectively.

After the via holes have been etched a Ti–Au–Ti electroplating base is sputtered onto the wafer, followed by coating with AZ4620. As a result the photoresist pools in the etched via holes and must be removed prior to electroplating. We inserted a via clear step at this point to facilitate photoresist removal. The via clear exposes only the photoresist in the via holes which is then developed out of the via hole. The remaining photoresist is now exposed with the microstrip pattern and developed. The wafer, which now has the microstrip pattern and cleared via holes on the backside, is electroplated with 4 μm of Au.

This procedure was used to fabricate a variety of CPW discontinuities, calibration standards, and the coplanar-to-microstrip transition.

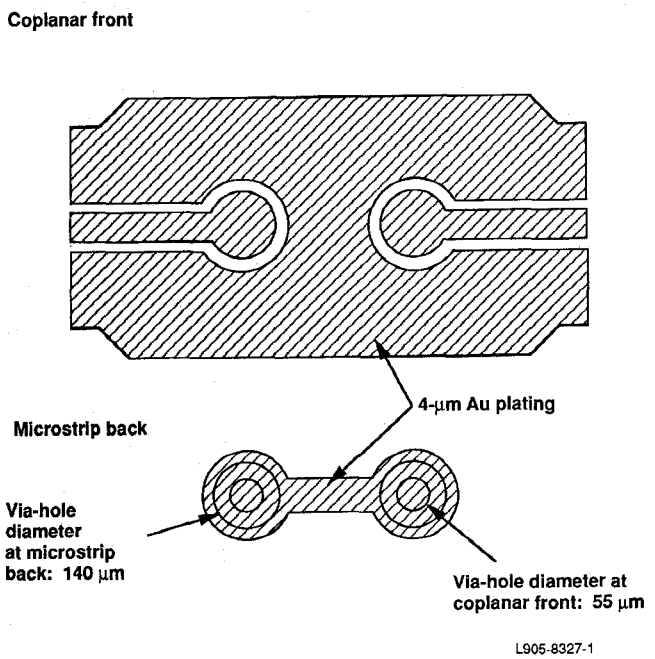

Fig. 1. Coplanar-to-microstrip transition.

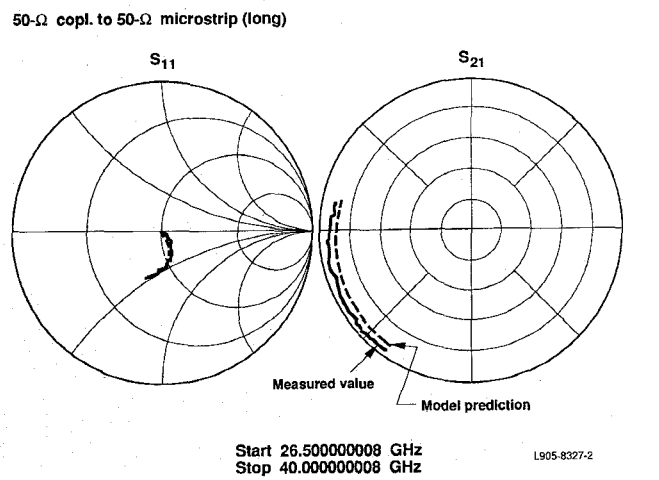

Fig. 2. On-wafer s-parameter measurement of a coplanar-to-microstrip transition.

III. Results and Discussion

Since coplanar circuit elements are not as well characterized as microstrip elements, we incorporated a variety of them on our mask set for fabrication. These structures included stubs, gaps, steps, tees and crosses of varying dimensions, all of which were fabricated for on-wafer test to 40 GHz with a Cascade wafer probe system.

Fig. 1 shows a typical passive element test structure in which the Cascade probing pads on the front side (CPW) are connected with via holes to microstrip on the backside. Measurements performed on-wafer to 40 GHz for a typical coplanar-to-microstrip transition are shown in Fig. 2. Again, we see very good agreement between our model and measured data. Each coplanar-to-microstrip transition has a measured loss of 0.15 dB at Ka-band, consistent with a via-hole resistance at RF of 0.5 ohm. The lumped-element equivalent circuit

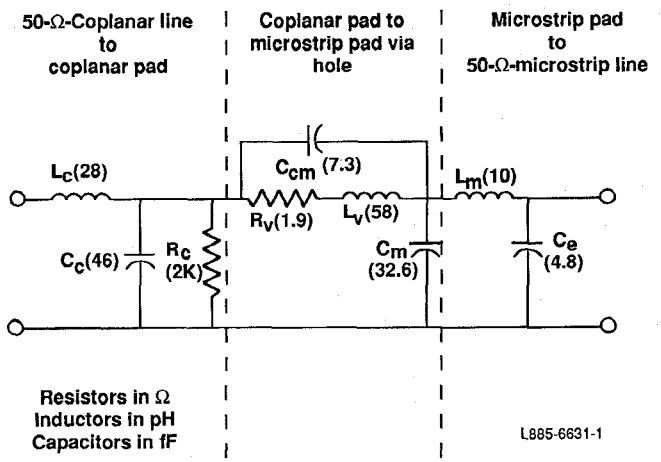

Fig. 3. Lumped-element equivalent circuit for a coplanar-to-microstrip transition.

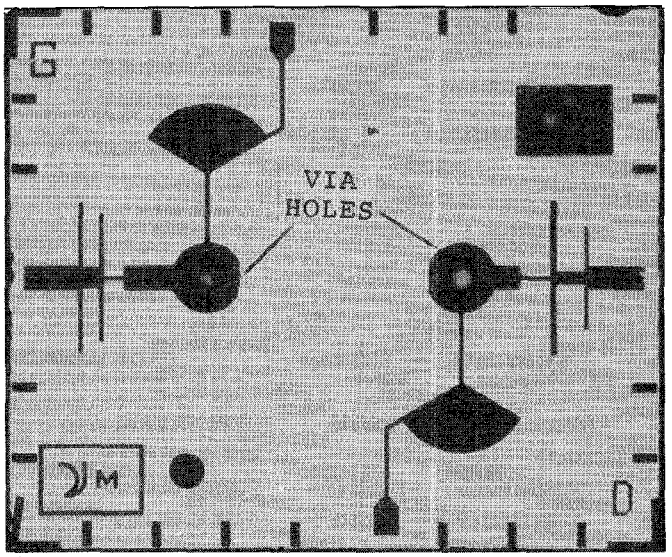

Fig. 4. W-band amplifier showing the microstrip input and output matching and biasing networks on the backside side of the wafer.

for the coplanar-to-microstrip transition is shown in Fig. 3.

The data obtained from measurements on the various CPW circuit elements and on the coplanar-to-waveguide transition were used to design a single-stage W-band amplifier [4]. This design capitalized on the strengths of the CPW and microstrip environments by 1) embedding the FET in CPW for low parasitics and 2) using via holes in series with the FET's gate and drain terminals to tune out the corresponding capacitance and to connect to microstrip matching networks on the opposite side, as shown in Fig. 4.

Scalar measurements performed on the amplifier between 90 and 100 GHz presented in Fig. 5 show a peak gain of 4.5 dB at 92 GHz together with the corresponding input return loss. The measured gain was in good agreement with our model prediction and compares well to the fully coplanar design fabricated at the same time which had a measured gain of 5.0 dB. At present our fully coplanar low noise amplifier designs have gains of 8.5 dB at 94 GHz and a 3.9-dB noise figure. The good agreement achieved between modeled and measured

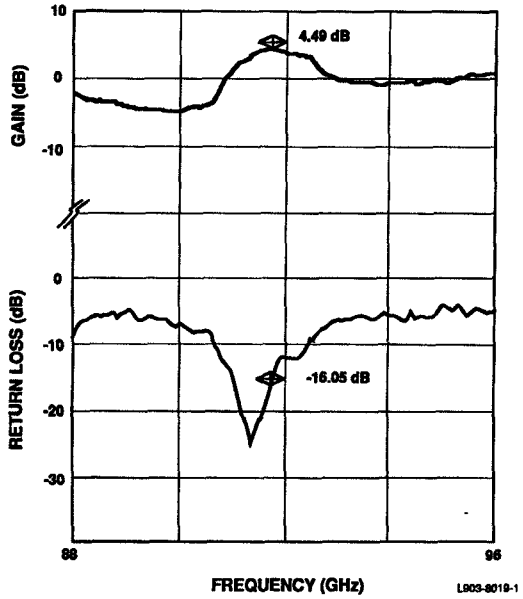

Fig. 5. Gain and return loss for a single stage W-band amplifier.

data together with the comparable performance with the first fully coplanar amplifier design demonstrates the viability of our coplanar-to-microstrip transition approach for fabricating W-band circuits.

IV. Conclusion

We have developed a technique for realizing W-band circuits in which the active device is placed in the coplanar waveguide line and matching elements in microstrip on the opposite side of the wafer. Accurate models of the various structures were developed and confirmed by on-wafer measurement to 40 GHz. We confirmed the viability of this approach by fabricating an amplifier with a gain comparable to a fully coplanar design of the same generation.

References

[1] P. A. Rizzi, *Microwave Engineering Passive Circuits*. Englewood Cliffs, NJ: Prentice Hall, 1988.

[2] M. E. Goldfarb and R. A. Pucel, "Modeling via hole grounds in microstrip," *IEEE Microwave Guided Wave Lett.*, vol. 1, pp. 135–137, June 1991.

[3] D. G. Swanson, Jr., "Grounding microstrip lines with via holes," *IEEE Trans. Microwave Theory Tech.*, vol. 40, pp. 1719–1721, Aug. 1992.

[4] H. B. Sequeira, S. W. Duncan, A. Eskandarian, B. A. Golja, D. C. Martel, S. B. Southwick, S. P. Svensson, M. W. Trippe, D. W. Tu, S. Weinreb, and N. E. Byer, "Monolithic GaAs W-band pseudomorphic MODFET amplifier," in *1990 GaAs IC Symp. Tech. Dig.*, Oct. 7–10, 1990.